AMENDMENT TO CLAIMS

The following listing of claims replaces all prior listings of claims in the application:

WHAT IS CLAIMED IS:

1. (Original) A memory comprising:

at least one data storage area comprising a plurality of data storage locations;

an access circuitry for accessing the data storage locations for retrieving or altering a data content thereof; and

at least one first user-configurable flag element and a second user-configurable flag element associated with said storage area, the first and second flag elements being used to define a protected state of the data storage area against alteration of the content of the data storage locations thereof, the protected state defined by the at least one first flag element being user-removable, while the protected state defined by the second flag element being permanent and non-removable.

2. (Original) The memory of claim 1, in which said second flag element can be set to define the permanent protected state of the respective data storage area irrespective of the fact that the at least one first flag element is set to define the removable protected state.

3. (Currently Amended) ~~The~~ A memory ~~of claim 1,~~ comprising:

at least one data storage area comprising a plurality of data storage locations;

an access circuitry for accessing the data storage locations for retrieving or altering a data content thereof; and

at least one first user-configurable flag element and a second user-configurable flag element associated with said storage area, the first and second flag elements being used to define a protected state of the data storage area against alteration of the content of the data storage locations thereof, the protected state defined by the at least one first flag element being user-

removable, while the protected state defined by the second flag element being permanent and non-removable,

in which the at least one first flag element has a first state and a second state, in which any alteration of the data content of the respective data storage area is allowed and, respectively, inhibited, and

the second flag element has a first state and a second state, in which changing of the state of the first flag element from the second state to the first state is allowed and, respectively, inhibited, so that when the second flag element is in the second state the respective data storage area is permanently protected against alteration of the data content thereof.

4. (Original) The memory of claim 1, in which the at least one first flag element comprises a non-volatile programmable and erasable storage element, and the second flag element comprises a one-time programmable non-volatile storage element.

5. (Original) The memory of claim 3, in which the second flag element can be set into the second state only if the at least one first flag element is in the second state.

6. (Original) The memory of claim 1, in which said at least one storage area comprises at least two storage areas, and in which for each of said at least two storage areas a respective first and second user-configurable flag elements are provided.

7. (Original) The memory of claim 1, comprising at least one further data storage area comprising a plurality of storage locations, and user-configurable flag means associated with said at least one further data storage area adapted to define a protected state of the at least one further data storage area against the alteration of the content of the respective storage locations, said protected state being removable by the user and not permanent.

8. (Original) The memory of claim 1, comprising means for conditioning the configuring of said first and second flag elements by the user on the recognition of the user by the memory.

9. (Original) A memory, comprising:

a first data-storage portion;

a first status portion corresponding to and operable to indicate first and second states of the first data-storage portion; and

a second status portion corresponding to and operable to indicate a third state of the first data-storage portion.

10. (Original) The memory of claim 9 wherein the second status portion is operable to indicate the third state only when the first status portion indicates the second state.

11. (Original) The memory of claim 9 wherein the second status portion is inoperable to indicate the third state when the first status portion indicates the first state.

12. (Original) The memory of claim 9, further comprising a second data-storage portion inoperable to be in the third state.

13. (Original) The memory of claim 9, further comprising a second data-storage portion inoperable to be in the second and/or third states.

14. (Original) The memory of claim 9, wherein the first state comprises a modifiable state.

15. (Original) The memory of claim 9, wherein the second state comprises a revocable unmodifiable state.

16. (Original) The memory of claim 9, wherein the third state comprises an irrevocable unmodifiable state.

17. (Original) A method, comprising:

receiving a request to modify a memory sector having a plurality of states; and

granting the request to modify if the sector is in a first state of the plurality, denying the request to modify if the sector is in a second and/or third state of the plurality.

18. (Original) A method, comprising:

receiving a request to transition a memory sector from a second or third state to a first state; and

granting the request to transition if the sector is in the second state, denying the request to transition if the portion is in the third state.

19. (Original) A method, comprising:

transitioning a memory sector to a revocable unmodifiable state; and

transitioning the memory sector to an irrevocable unmodifiable state only after transitioning the memory sector to the revocable unmodifiable state.

20. (Original) An electronic system, comprising:

a memory device, comprising:

a first data storage portion;

a first memory coupled and corresponding to the first portion, the first memory operable to indicate first and second states of the first portion; and

a second memory coupled to the first memory and corresponding to the first portion, the second memory operable to indicate a third state of the first portion.